CLAIMS

1. A memory package comprising:

a first circuit board having two faces, the first circuit board comprising a memory die on a first face of the circuit board and a controller die on the second face;

a second circuit board having two faces and an opening, the first face of the second circuit board affixed to the second face of the first circuit board such that the controller die is within the opening; and

vias connecting the memory die to the second face of the second circuit board, and connecting the memory die to the controller die.

2. The memory package of claim 1 further comprising solder balls on the second face of the second circuit board, the solder balls affixed to the vias.

3. The memory package of claim 1 further comprising a first encapsulant covering the memory die and a portion of the first circuit board.

4. The memory package of claim 1 further comprising a second encapsulant covering the controller die.

5. The memory package of claim 1 wherein the thickness of the package is about 0.7 millimeters.

6. The memory package of claim 2, wherein the thickness of the package including the solder balls is about 1.0 millimeters.

7. The memory package of claim 1 further comprising bond wires, the bond wires connecting the memory die and the controller die to the vias or a conductive layer of the first circuit board coupled to the vias.

8. The memory package of claim 1, wherein the memory die is conductively affixed to a conductive layer of the first circuit board without the use of bond wires.

9. The memory package of claim 1, wherein the controller die is conductively affixed to a conductive layer of the first circuit board without the use of bond wires.

10. The memory package of claim 1, wherein the memory is FLASH type memory.

11. The memory package of claim 1 further comprising a set of contacts on either the first or second circuit board, the set of contacts exposed.

12. A memory package comprising:

a circuit board having a first and second face, the second face having a recess;

a memory die attached to the first face of the circuit board, the memory die positioned above the recess;

a controller die attached to and positioned within the recess of the second face of the circuit board, the second face of the circuit board forming a second face of the package; and

vias connecting the memory die to the second face of the circuit board.

13. The memory package of claim 12 further comprising bond wires, the bond wires connecting the memory die and the controller die to the vias or a conductive layer of the circuit board coupled to the vias.

14. The memory package of claim 12, wherein the memory die is conductively affixed to a conductive layer of the circuit board without the use of bond wires.

15. The memory package of claim 12, wherein the controller die is conductively affixed to a conductive layer of the circuit board without the use of bond wires.

16. The memory package of claim 12, wherein the memory is FLASH type memory.

17. The memory package of claim 12 further comprising a set of contacts on a face of the circuit board.

18. The memory package of claim 17 wherein the contacts are on the second face of the circuit board.

19. The memory package of claim 17 further comprising an encapuslent around the first face and edges of the package.

20. The memory package of claim 18, further comprising a plastic covering over the first and second face and the edges of the package.

21. A method of making a memory package comprising:

attaching a plurality of memory die to the first face of a first circuit board;

attaching a plurality of controller die to the second face of the first circuit board, each controller die positioned beneath a memory die;

laminating the second face of the first circuit board to a first face of a second circuit board having a plurality of recesses such that the plurality of controller die fit within the plurality of recesses;

forming vias in the first and second circuit boards connecting the controller die to beneath the memory die to the memory die to form a plurality of memory packages; and

cutting the first and second circuit boards between the plurality of memory packages to form individual memory packages.

22. A memory card comprising:

a first circuit board having a first and second face;

a memory package comprising a second circuit board, a controller die attached to a first face of the second circuit board, and a memory die attached to a second face of the second circuit board, and wherein

the memory package is attached to the first face of the first circuit board; and

a set of contacts on the second face of the first circuit board.

23. The memory card of claim 22 further comprising a set of circuit traces within the first circuit board coupled to the memory die, controller die, and the set of contacts.

24. The memory card of claim 23 wherein the circuit traces are coupled to the memory die, controller die, and the set of contacts with vias.

25. The memory card of claim 22 further comprising a cover extending over the first face and edges of the circuit board.

26. The memory card of claim 25 wherein the cover further extends over the second face of the circuit board, the cover having openings for the set of contacts.

27. A microprocessor controlled device comprising:

a memory chip package comprising a circuit board having a first and second face, a controller die attached to the first face, and a memory die attached to the second face;

one or more input-output devices;

random access memory; and

a microprocessor.

28. A memory chip package comprising:

a circuit board having first and second opposing faces;

a FLASH EEPROM having memory cells, the EEPROM attached to the first face of the circuit board;

a controller having a control logic, the controller attached to the second face of the circuit board and configured to read and write data to the memory cells on the first face; and

data lines connecting the controller die to the EEPROM and operable to transfer data to and from the memory cells.

29. The memory chip package of claim 28 wherein the controller further comprises:

a microprocessor;

a memory buffer; and

a system interface.

30. The memory chip package of claim 28 further comprising:

address lines connecting the memory cells on the first face to the controller on the second face, the address lines operable to address one or more memory cells for the reading and writing of the data.

31. The memory chip package of claim 30 further comprising:

control and status lines connecting the memory cells on the first face to the controller on the second face, the control and status lines operable to monitor the state of the memory cells over the control and status lines.